PC Engines

ALIX.2 / ALIX.3 series system boards

PC Engines GmbH
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Federal Communications Commission Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio energy. If this equipment is not installed and used in accordance with the manufacturer's instructions, it may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment to an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

This board is designed for installation in a shielded enclosure (metal or plastic with conductive coating). Shielded cables are required on LAN and serial ports to assure compliance with FCC regulations.

A copy of the test report will be provided on request.

CE Declaration of Conformity

We, PC Engines GmbH, declare that ALIX.2 and ALIX.3 series boards, when installed in PC Engines metal enclosures. (case1c1 / case1c2 / box2c), are in conformance with:

- EN 61000-6-3 (2005) (emissions, residential and industrial)
- EN 61000-6-2 (ESD, susceptibility, residential and industrial)

The unit under test is in conformity with the standards mentioned above. A copy of the test report will be provided on request.

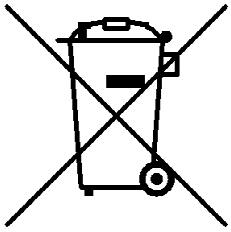
Compliance information

For FCC, ALIX has been tested as a CPU board, installed in an enclosure, with the top cover removed. No further testing should be required if the board is used with other FCC tested modular components. Please see http://www.fcc.gov/oet/ for more details. The responsible party for FCC is the importer.

Testing for CE mark must be done at the level of the complete product, possibly including the wireless cards. Please contact PC Engines for assistance and documentation.

For satisfactory resistance to electrostatic discharge events (ESD), the ALIX board should be grounded (e.g. through the mounting holes, or the serial port connector). The USB port on ALIX.2B / ALIX.3B boards is sensitive to ESD events, spurious overcurrent events may be detected in this version.

Recycling / disposal



Do not discard electronic products in household trash!

All waste electronics equipment should be recycled according to local regulations.

Information for the recycler:

Cut off Lithium battery, if present, for separate recycling.

PC Engines enclosures are made of aluminium.

Introduction / features

ALIX.2 and ALIX.3 are small form factor system boards optimized for wireless routing and network security applications.

- AMD Geode LX CPU, 433 Mhz (LX700) or 500 MHz (LX800) 5x86 CPU,
- 256 KB cache (64K data + 64K instruction + 128K L2)
- 1 to 3 Ethernet channels (Via VT6105M, 10 / 100 Mbit/s)
- 1 or 2 miniPCI sockets for 802.11 wireless cards and other expansion
- 128 or 256 MB DDR SDRAM, 64 bit wide for high memory bandwidth
- 512 KB flash for PC Engines tinyBIOS
- CompactFlash + optional 44 pin IDE header for user's operating system and application
- 7 to 18V (absolute maximum) DC supply through DC jack or passive power over Ethernet
- 1 serial port (DB9 male)
- 2 USB 2.0 ports (optional)
- Header for LPC bus (use for flash recovery or I/O expansion)

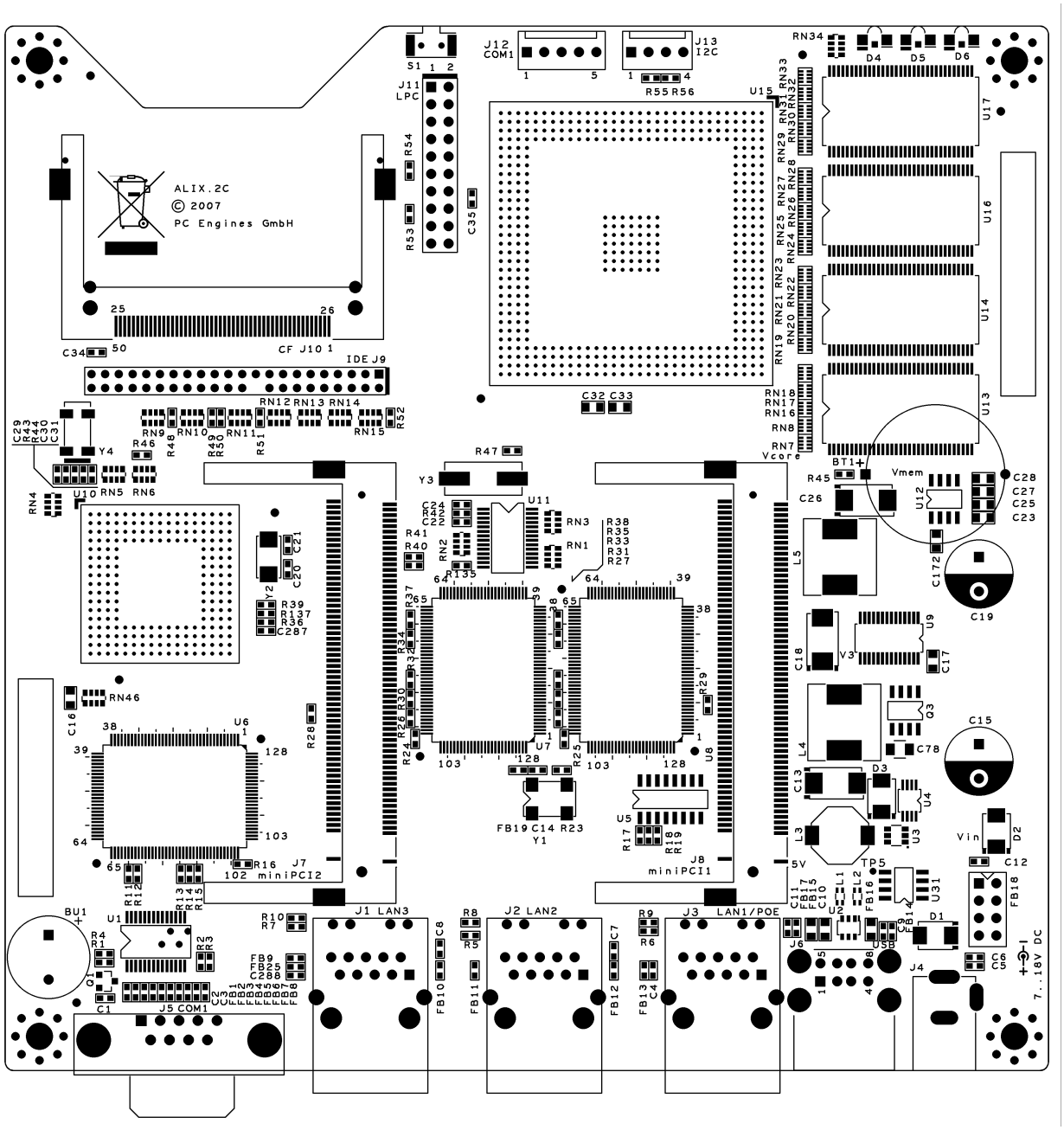
OEM options

The following options can be configured for larger orders:

- DRAM size (128 MB, 256 MB)
- CPU speed (LX700 / LX800 / LX900)
- Delete I/O not required by customer
- CMOS level serial port (RXD / TXD only)
- Optional header for I2C bus
- Optional buzzer for "beeps"
- Optional RTC battery
- ALIX.3: optional AC97 audio codec (headphone + mic)
- ALIX.3: optional VGA video
- ALIX3: optional pushbutton switch
- PC Engines tinyBIOS

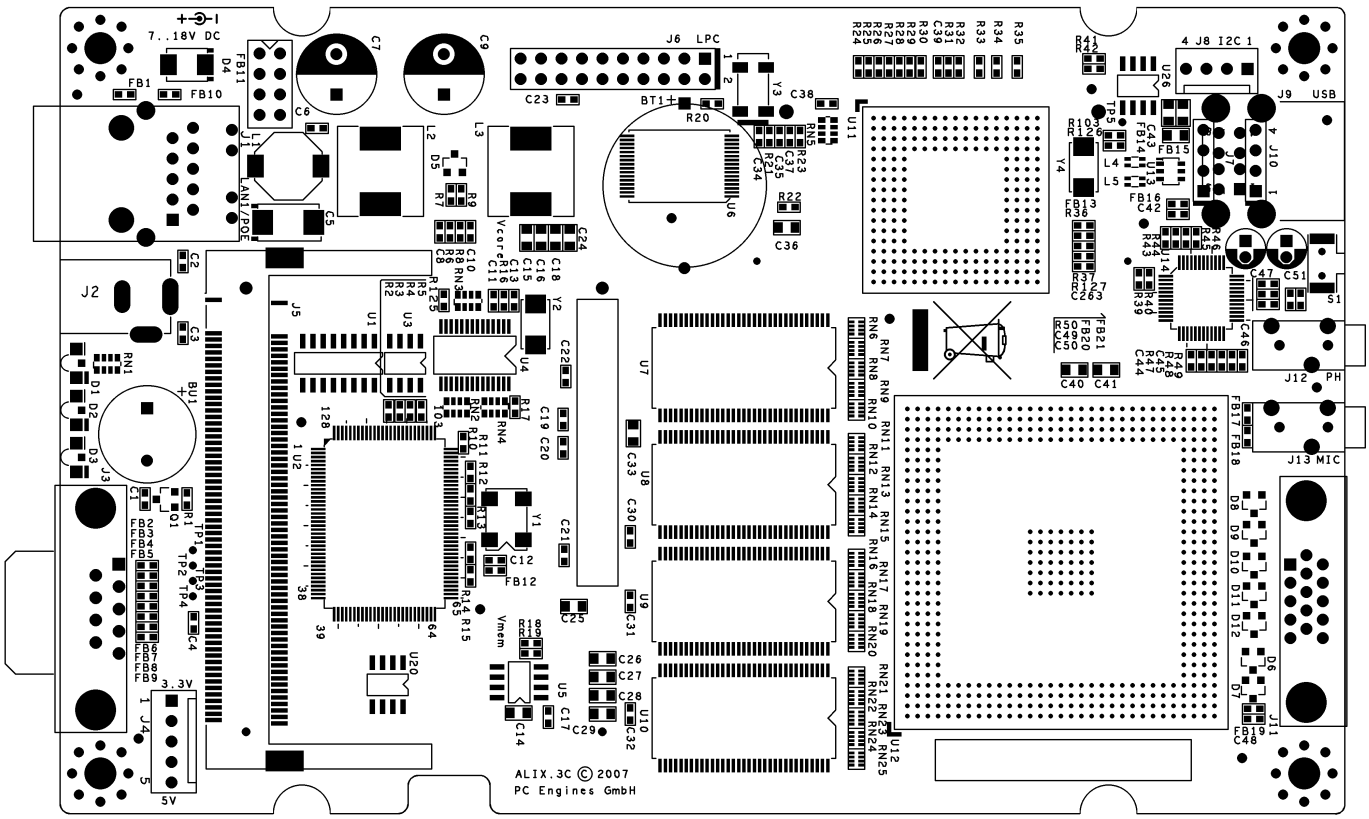
ALIX.2 series

Configuration	2 LAN / 2 miniPCI, or 3 LAN / 1 miniPCI
Power supply	7 to 20V DC, about 3 to 4W at Linux idle, peak about 6W without miniPCI cards and USB devices. Suggest a 18V / 15W supply. Center pin = positive, sleeve = ground, 2.1 mm diameter.
Temperature range	0 to 50°C.
Dimensions	6 x 6" (152.4 x 152.4 mm)



ALIX.3 series

Configuration	1 LAN / 2 miniPCI
Power supply	7 to 20V DC, about 2.5 to 3.5W at Linux idle, peak about 5W without miniPCI cards and USB devices. Suggest a 18V / 15W supply. Center pin = positive, sleeve = ground, 2.1 mm diameter.
Temperature range	0 to 50°C.
Dimensions	100 x 160 mm



Getting started…

- Install a bootable CF card. Hot swap of CF cards is not supported!
- Connect serial port to a PC through null modem cable (RXD / TXD crossed over). Set terminal emulator to 38400 8N1, flow control = none or xon-xoff.
- Connect Ethernet as needed.
- Connect a 18V DC power supply to the DC jack. Power supply should be able to supply at least 12W for some margin. To avoid arcing, please plug in the DC jack first, then plug the adapter into mains.

The board should now power on. All three LEDs will light during BIOS POST, then the system will try to boot, and turn off two of the LEDs.

You should see tinyBIOS startup messages, memory size, CF disk geometry on the serial console.

Setup options

To enter setup, type S during the memory test. You should see something like the following:

```
PC Engines ALIX.2 v0.98j
640 KB Base Memory
261120 KB Extended Memory

01F0 Master 848A CF 128MB
Phys C/H/S 1002/8/32 Log C/H/S 1002/8/32

BIOS setup:

(9) 9600 baud (2) 19200 baud *3* 38400 baud (5) 57600 baud (1) 115200 baud
*C* CHS mode (L) LBA mode (W) HDD wait (V) HDD slave (U) UDMA enable
(M) MFGPT workaround
(P) late PCI init
*R* Serial console enable
(E) PXE boot enable
(X) Xmodem upload
(Q) Quit
```

9 sets baud rate to 9600 baud
2 sets baud rate to 19200 baud
3 sets baud rate to 38400 baud
4 sets baud rate to 57600 baud
1 sets baud rate to 115200 baud

C sets CF / HDD to CHS mode
L sets CF / HDD to LBA mode
W toggles HDD delay – HDD takes more time to spin up
V toggles HDD slave – HDD slave detection takes time, normally disabled
U toggles UDMA enable – use at your own risk

M toggles MFGPT workaround – may be required to support high speed timer. See AMD CS5536 data book section 5.16.3 for the gory details. The system may hang during boot if you get it wrong…

P toggles late PCI init – use for FPGA based miniPCI cards that take a long time to come up. Symptom: no interrupt assigned.

R toggles serial console enable. Push the switch S1 during startup to get into setup when the serial console is disabled.

E toggles PXE boot enable. Defaults to disable as the PXE module has a 60 second time-out.

X Xmodem upload – start upload of an executable binary. Intended for flash BIOS update, ask for more information if necessary.

Q quit – asks whether to write back the changes to flash (Y) or not (N). Then the system will restart.

PXE boot

PXE boot can be activated either through the E option in setup (always), or by pressing N during memory test (one time). PC Engines cannot provide technical support for the PXE module, too many possible failure points (Intel / Via PXE module, DHCP server, TFTP server, boot image etc).

Power over Ethernet

ALIX implements a passive power over Ethernet scheme, using the unused pairs of LAN1 for power. Power can be injected using a passive POE splitter such as PC Engines POE.1A.

When power is fed in through POE, it is possible to "steal" unregulated power through the DC jack. Please note that this port is not fused. The POE input diode is rated for a current of 2A. Please keep in mind that any EMI energy injected on this port will go out through the Ethernet cable without filtering.

Operating system compatibility

Please keep in mind that ALIX.2 and ALIX.3 boards do not include a keyboard controller. Some boot loaders may hang and need to be modified.

For best performance, include support for AMD Geode LX / CS5536, and use a current driver for the Via VT6105M LAN controller (supports TCP/IP checksumming, byte aligned transmit buffers).

Reboot is best triggered by port 92h.

FreeBSD

Current versions of FreeBSD may panic due to issues in the EHCI configuration. Disable EHCI driver if problems appear.

FreeDOS, MS-DOS 5.0

Tested ok, booting from CF card.

Linux

Try www.imedialinux.com for a kernel preconfigured with Geode LX drivers.

NetBSD

Not yet tested.

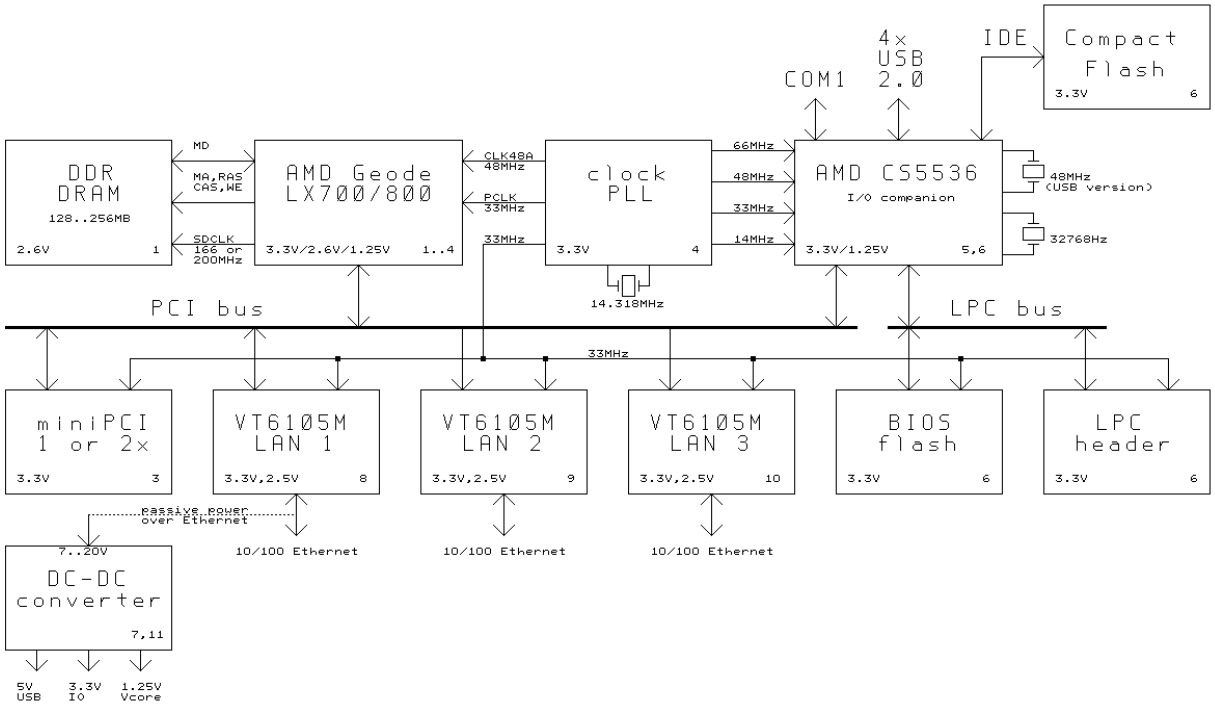
OpenBSD

OpenBSD 4.0-stable and later versions should support AMD Geode LX.

GPIO supported by glxpcib(4) driver.

ALIX block diagram

Schematics will be made available to qualified customers.



ALIX connector pinouts

References refer to ALIX.2 / ALIX.3.

J5/J3 COM1 serial port

The standard PC pinout is used. To connect to a PC, use a null modem or "Laplink" cable. Due to limitations of the AMD CS5536 companion chip, handshake signals are not available.

1	DCD	data carrier detect (input)	- not available on CS5536
2	RXD#	receive data (input)	
3	TXD#	transmit data (output)	
4	DTR	data terminal ready (output)	- driven active
5	GND	ground	
6	DSR	data set ready (input)	- not available on CS5536
7	RTS	ready to send (output)	- driven active
8	CTS	clear to send (input)	- not available on CS5536
9	RI	ring indicator (input)	- not available on CS5536

J12 / J4 COM1 serial port (build option)

As an option, the board can be configured with a 4 or 5 pin header with 3.3V CMOS signal levels instead of the normal RS-232 serial port.

1	V3	3.3V supply
2	TXD	transmit data (output)
3	RXD	receive data (input)
4	GND	ground
5	VCC	5V supply

J3/J1 Ethernet port 1

RJ45 connectors with integrated magnetics are used. This port implements a passive power over Ethernet scheme over the two unused pairs. Do not exceed 20V as the TVS protection diode may start clamping above this voltage.

1	TX+	transmit positive
2	TX-	transmit negative
3	RX+	receive positive
4	VIN	power supply (nominal 7 to 20V)
5	VIN	"
6	RX-	receive negative
7	GND	power return
8	GND	"

J1, J2 / - Ethernet ports 2, 3

RJ45 connectors with integrated magnetics are used. These ports do NOT support power over Ethernet. Same pinout as above, but pins 4,5 and 7,8 are not connected.

J6/J9 USB jack (build option)

Dual USB 2.0 connections:

1	VCC	switched +5V supply
2	DATA4-	negative data
3	DATA4+	positive data
4	GND	ground
5	VCC	switched +5V supply
6	DATA3-	negative data
7	DATA3+	positive data
8	GND	ground

J4/J2 DC power jack

This is a generic DC jack connector with a 2.1mm center pin. Recommended input voltage is +18V.

center	VIN	Positive input voltage
sleeve	GND	Ground

J7, J8 / J5, J14 miniPCI socket

These sockets implement the miniPCI interface. Please see schematic for pinout.

J9 / - IDE header (build option)

1	HDRST#	IDE reset
2	GND	ground
3	HDD7	IDE data 7
4	HDD8	IDE data 8
5	HDD6	IDE data 6
6	HDD9	IDE data 9
7	HDD5	IDE data 5
8	HDD10	IDE data 10
9	HDD4	IDE data 4
10	HDD11	IDE data 11
11	HDD3	IDE data 3
12	HDD12	IDE data 12
13	HDD2	IDE data 2
14	HDD13	IDE data 13
15	HDD1	IDE data 1
16	HDD14	IDE data 14
17	HDD0	IDE data 0
18	HDD15	IDE data 15
19	GND	ground
20	key	key pin (missing)
21	HDRQ	IDE DMA request
22	GND	ground
23	HDIOW#	IDE I/O write
24	GND	ground
25	HDIOR#	IDE I/O read
26	GND	ground
27	HDIORDY	IDE I/O ready
28	CSEL	cable select (pull down)

29	HDACK#	IDE DMA acknowledge
30	GND	ground
31	HDIRQ	IDE interrupt
32	nc	no connect
33	HDA1	IDE address 1
34	HDPDIA#	IDE diagnostic, 80 pin cable ID
35	HDA0	IDE address 0
36	HDA2	IDE address 2
37	HDCS0#	IDE chip select 0
38	HDCS1#	IDE chip select 1
39	HDLED#	IDE led output
40	GND	ground
41	VCC	5V power
42	VCC	5V power
43	GND	ground
44	GND	ground

J10 / J15 CompactFlash

The CompactFlash card is used in True IDE mode. Hot insertion is not supported – please power off the unit before inserting a CF card.

1	GND	ground
2	D3	IDE data
3	D4	IDE data
4	D5	IDE data
5	D6	IDE data
6	D7	IDE data
7	CS0#	IDE decode (1F0..1F7)
8	A10	ground
9	ATASEL#	ground to select true IDE mode
10	A9	ground
11	A8	ground
12	A7	ground
13	VCC	+3.3V power supply
14	A6	ground
15	A5	ground
16	A4	ground
17	A3	ground
18	A2	IDE address
19	A1	IDE address
20	A0	IDE address
21	D0	IDE data
22	D1	IDE data
23	D2	IDE data
24	IO16#	16 bit decode, not connected
25	CD2#	card detect, not connected
26	CD1#	card detect. not connected
27	D11	IDE data
28	D12	IDE data
29	D13	IDE data
30	D14	IDE data

31	D15	IDE data
32	CS1#	IDE decode (3F6..3F7)
33	VS1#	not connected
34	IOR#	IDE read strobe
35	IOW#	IDE write strobe
36	WE#	connected to +3.3V
37	IRQ	IDE interrupt
38	VCC	+3.3V power supply
39	CSEL#	cable select, ground = master
40	VS2#	not connected
41	RESET#	IDE reset, active low
42	IORDY	IDE ready
43	INPACK#	IDE DMA request
44	REG#	IDE DMA acknowledge
45	DASP#	pulled up
46	PDIAG#	pulled up
47	D8	IDE data
48	D9	IDE data
49	D10	IDE data
50	GND	ground

The CompactFlash specification can be found at www.compactflash.org.

J11 / J6 LPC expansion

The LPC port is used in the factory to connect an alternate flash BIOS to start the board when the on-board flash is corrupted or blank. Use PC Engines adapter LPC.1A for this purpose if needed.

The LCP port can also be used to connect a super I/O device. Unlike SC1100 based WRAP boards, this port cannot be reprogrammed as GPIO pins.

1	LCLK0	LPC clock (33 MHz)
2	GND	ground
3	LAD0	LPC data 0
4	GND	ground
5	LAD1	LPC data 1
6	GND	ground
7	LAD2	LPC data 2
8	GND	ground
9	LAD3	LPC data 3
10	GND	ground
11	LFRAME#	LPC frame
12	GND	ground
13	PCIRST#	reset (active low)
14	CLK48	super I/O clock (48 MHz)
15	ISP	high to use LPC flash, low to use on-board flash, pulled low by resistor
16	VCC	+5V supply
17	GND	ground
18	V3	+3.3V supply
19	SERIRQ	serial interrupt
20	LDRQ#	LPC DMA request

J13 / J8 **I2C bus (build option)**

This optional header can be used to connect user specific hardware, e.g. a front panel microcontroller, or for a licensing dongle. See AMD CS5536 data sheet for programming details.

1	+3.3V	power supply
2	SMB_SCL	I2C clock
3	SMB_SDA	I2C data
4	GND	ground

- / J12 **Headphone out (build option)**

- / J13 **Microphone in (build option)**

- / J11 **VGA (build option)**

1	VGAR	VGA red
2	VGAG	VGA green
3	VGAB	VGA blue
4	nc	no connect
5	GND	ground
6	GND	ground
7	GND	ground
8	GND	ground
9	USBVCC	+5V supply (fused)
10	GND	ground
11	nc	no connect
12	DDCDAT	DDC data
13	HS	horizontal sync
14	VS	vertical sync
15	DDCCLK	DDC clock

BT1 **RTC battery (build option)**

Footprint for CR2032 Lithium battery. Please observe correct polarity, top side of the battery is + positive terminal. Specification: CR2032, horizontal mount, 20.4 mm lead spacing, for example:

Renata CR2032FH1

Panasonic BR2032-1HE

BU1 **Buzzer (build option)**

Optional speaker. Driver circuit not populated, please contact PC Engines for instructions if you would like to add this.

Status LEDs

Status LEDs are all turned on by the BIOS on power up. The BIOS will turn off LEDs 2 and 3 before booting the operating system.

Location	GPIO	read port	write port
LED1 (left)	G6	port 06100h bit 6	port 06100h bit 6 / 22
LED2 (middle)	G25	port 06180h bit 9	port 06180h bit 9 / 25
LED3 (right)	G27	port 06180h bit 11	port 06180h bit 11 / 27

The CS5536 GPIO ports are programmed by 32 bit atomic writes. This avoids the need for read / modify / write operations and the locking issues they entail. For example, to turn off LED1 (high), write 0000'0040h to port 06100h. To turn on LED1 (low), write 0040'0000h. Multiple port bits can be changed at the same time.

Mode switch

The mode switch can be accessed by software as follows:

Location	GPIO	read port	
MODESW#	G24	port 061b0h bit 8	(active low, 0 = switch pressed)

BIOS POST codes

tinyBIOS writes POST / diagnostic codes to port 80h. To make these codes visible, use a miniPCI POST card such as PC Engines POST.5A. POST codes are:

01	reset entry
02	chipset initialization
03	detect base memory size
04	initialize shadow RAM
05	init mono video
06	disable PCI devices
07	test low 64KB of DRAM
08	initialize stack
09	BIOS checksum
0a	super I/O initialization
0b	RTC test
0c	refresh / 8254 test
0d	speed-dependent chipset regs
0e	test 8237 DMA
0f	test DMA page registers
10	test 8254 registers
11	test keyboard controller
12	init timer, DMA, 8259...
13	test 8259 mask registers
14	test low 640KB
15	init vectors
16	PCI plug & play
17	shadow video BIOS
18	look for VGA BIOS
19	sign-on prompt
1a	second keyboard test
1b	extended memory test
1c	enable interrupts
1d	test / init RTC
1e	init floppy disk
1f	option ROM scan
20	test parallel ports
21	test serial ports
22	enable coprocessor
23	floppy init
24	hard disk init
25	PS/2 mouse detect
26	timer/RTC check
27	OEM boot decision point
00	boot
33	NMI
F7	low 64KB memory test failed